

APPLICANT(S): VINITZKY, Gil
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FILED: December 28, 2001
Page 2

AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

Claim 1. (Currently Amended) A method for indexing a plurality of ordered elements stored in bit-reversed order in a first memory space and a separate second memory space, wherein said first memory space is indexed by a first memory index denoting the memory positions in said first memory space, wherein said second memory space is indexed by a second memory index denoting the memory positions in said second memory space, and wherein the logical position of each of said elements within said plurality of ordered elements is indexed by an element index, the method comprising:

- bit-reversing the element index of a selected one of said elements;
- locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and
- locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

Claim 2. (Original) A method according to claim 1 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s , and wherein said element index comprises t digits where n equals 2^t .

APPLICANT(S): VINITZKY, Gil
SERIAL NO.: 10/028,938
FILED: December 28, 2001
Page 3

Claim 3. (Cancelled)

Claim 4. (**Currently Amended**) A Digital Signal Processing architecture capable of storing a plurality of ordered elements in bit-reversed order in a first memory space and a separate second memory space, the architecture comprising:

- a first memory index denoting the memory positions in said first memory space;

- a second memory index denoting the memory positions in said second memory space;

- an element index denoting the logical position of each of said elements within said plurality of ordered elements;

- means for bit-reversing the element index of a selected one of said elements;

- means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and

- means for locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

Claim 5. (Original) An architecture according to claim 4 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s , and wherein said element index comprises t digits where n equals 2^t .

Claim 6. (Original) An architecture according to claim 4 and further comprising means for creating any of said indices.

Claim 7. (Cancelled)

APPLICANT(S): VINITZKY, Gil
SERIAL NO.: 10/028,938
FILED: December 28, 2001
Page 4

Claim 8. (Currently Amended) A Digital Signal Processor comprising:

a first memory space and a separate second memory space collectively capable of storing a plurality of ordered elements in bit-reversed order;

first memory indexing means operative to denote in a first memory index the memory positions in said first memory space;

second memory indexing means operative to denote in a second memory index the memory positions in said second memory space;

element indexing means operative to denote in an element index the logical position of each of said elements within said plurality of ordered elements; and

processing means comprising:

means for bit-reversing the element index of a selected one of said elements;

means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and

means for locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

Claim 9. (Original) A processor according to claim 8 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s , and wherein said element index comprises t digits where n equals 2^t .

Claim 10. (cancelled)